CLAIMS

I claim:

1 A memory system including a control path to a host device supplying a voltage, comprising:

a voltage regulator including an input, an output and a bypass shorting the input to the output;

a voltage detector communicating with the regulator;

a bypass enable signal operable responsive to a signal generated by the host device indicating that the power up of the host is complete.

2. The memory system of claim 1 further including a voltage detector outputting a signal indicative of the host supply voltage.

3. The memory system of claim 1 wherein the bypass is at least one transistor.

4. The memory system of claim 3 wherein the bypass comprises a plurality of transistors.

5. The memory system of claim 3 wherein the bypass enable signal is provided by the controller to a gate of the transistor.

6. The memory system of claim 1 wherein the signal generated by the host device is a command signal to the memory system.

7. The memory system of claim 1 wherein the memory system is a multimedia card.

8. The memory system of claim 1 wherein the memory system is a multimedia card and the signal generated by the host device is a command signal.

9. The memory system of claim 8 wherein the command signal is CMD0 or CMD1.

10. The memory system of claim 1 wherein the signal generated by the host is a signal indicating power up of the host device is complete.

11. The memory system of claim 1 wherein the memory system is a pc card.

12. The memory system of claim 1 wherein the memory system is a compact flash card.

13. The memory system of claim 1 wherein the memory system is a secure digital card.

14. The memory system of claim 1 wherein the memory system is a smart media card.

15. The memory system of claim 1 wherein the memory system is a memory stick.

16. A method for operating a voltage regulator in a memory system, comprising:

providing a voltage regulator having an input and an output, and including a regulator bypass shorting the input to the output;

setting the bypass to off prior to power up of a host device;

responsive to a power up completion signal from a host device, determining the power supplied by the host; and

if the power is below a threshold operating voltage, enabling the bypass.

17. The method of claim 16 wherein the bypass is a transistor and the step of setting the bypass to off includes providing a signal to a gate of the transistor.

18. The method of claim 17 wherein the bypass comprises a plurality of transistors and the step of enabling the bypass comprises applying an enable signal to each gate of said plurality of transistors.

19. The method of claim 17 wherein the power up completion signal is a command signal from the host.

20. The method of claim 19 wherein command signal is CMD0 or CMD1 for a multimedia card.

21. The method of claim 17 wherein the threshold voltage is below 2.7 volts.

22. The method of claim 17 wherein the threshold voltage is below 2.0 volts.

23. The method of claim 17 wherein the threshold voltage is below 1.65 volts.

24. The method of claim 17 wherein the threshold voltage is below 1.3 volts.

25. A peripheral device for a host system including a voltage regulator circuit, comprising:

a voltage regulator having an input and an output;

a bypass element coupled to selectively short the input to the output;

a bypass control signal coupled to the bypass element and responsive to a host system power up completed signal which enables the bypass element when the voltage provided by the host is below a threshold level.

26. The peripheral device of claim 25 wherein the regulator includes a detector responsive to the power up completed signal.

27. The peripheral device of claim 26 wherein the detector outputs a first signal when the voltage provided by the host is above a threshold and a second signal when the host is below a threshold.

28. The peripheral device of claim 25 wherein the bypass element includes at least one p-type transistor.

29. The peripheral device of claim 27 wherein the bypass control signal is applied to the gate of the at least one transistor.

30. The peripheral device of claim 27 wherein the bypass element is disabled during power up of the host device.

31. The peripheral device of claim 25 wherein the bypass control signal is provided by a controller.

32. A method for operating a voltage regulator in a multimedia card memory device, comprising:

providing a voltage regulator having an input and an output, and including a regulator bypass shorting the input to the output;

setting the bypass to off prior to power up of a host device;

responsive to a command signal from the host device, determining the power supplied by the host; and

if the power is below a threshold operating voltage, enabling the bypass.

33. The method of claim 19 wherein command signal is CMD0 or CMD1 in for a multimedia card.

34. A memory system, comprising:

a controller;

a memory array; and

a voltage regulator having a shorting element between an input and an output responsive to a bypass control signal, the bypass control signal provided by the controller responsive to a host system power up complete signal which enables the bypass element when a host supply voltage provided by the host is below a threshold level.

35. The memory system of claim 34 wherein the regulator outputs a voltage less than the host supply voltage when said supply voltage is above said threshold.

36. The memory system of claim 35 wherein the regulator outputs at least a first or a second output voltage when said host supply voltage is above said threshold.